ANALOG DEVICES

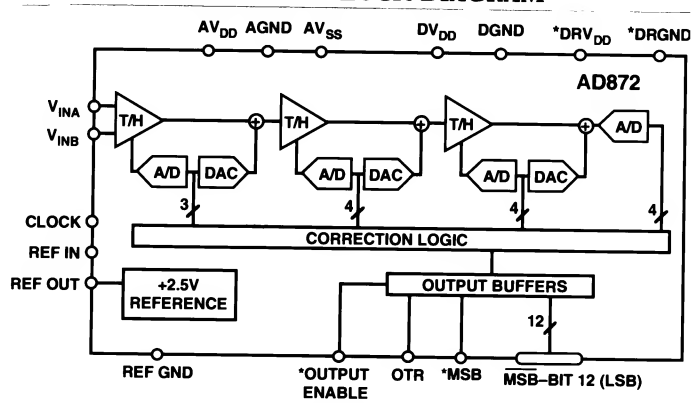
Complete 12-Bit 10 MSPS Monolithic A/D Converter

AD872

FEATURES

Monolithic 12-Bit 10 MSPS A/D Converter
Low Power Dissipation: 1.15 W
No Missing Codes Guaranteed
Differential Nonlinearity Error: 0.5 LSB
Complete: On-Chip Track-and-Hold Amplifier and Voltage Reference
Signal-to-Noise and Distortion Ratio: 65 dB
Spurious-Free Dynamic Range: 72 dB
Out of Range Indicator
Twos Complement Binary Output Data
28-Pin Ceramic DIP or 44-Pin Surface Mount Package

FUNCTIONAL BLOCK DIAGRAM



* ONLY AVAILABLE ON 44 PIN SURFACE MOUNT PACKAGE.

PRODUCT DESCRIPTION

The AD872 is a monolithic 12-bit, 10 Msps analog to digital converter with an on-chip, high performance track-and-hold amplifier and voltage reference. The AD872 uses a multistage differential pipelined architecture with output error correction logic to provide 12-bit accuracy at 10 Msps data rates and guarantees no missing codes over the full operating temperature range. The AD872 combines a merged high speed bipolar/CMOS process and a novel architecture to achieve the resolution and speed of hybrid implementations at a fraction of the power consumption. Additionally, the greater reliability of monolithic construction offers improved system reliability and lower costs than hybrid designs.

The high input impedance, fast-settling input track-and-hold (T/H) amplifier is equally suited for both multiplexed systems that switch negative to positive full-scale voltage levels in successive channels and sampling single-channel inputs at frequencies up to and beyond the Nyquist rate. The AD872's wideband input combined with the power and cost savings over previously available hybrids will allow new design opportunities in communications, imaging and medical applications. The AD872 provides both reference output and reference input pins, allowing the onboard reference to serve as a system reference. An external reference can also be chosen to suit the dc accuracy and temperature drift requirements of the application. A single clock input is used to control all internal conversion cycles. The digital output data is presented in twos complement binary output format. An out-of-range signal indicates an overflow condition. It can be used with the most significant bit to determine low or high overflow.

The AD872 is fabricated on Analog Devices ABCMOS-1 process which utilizes high speed bipolar and CMOS transistors on a single chip. High speed, precision analog circuits are now combined with high density logic circuits.

The AD872 is packaged in a 28-pin ceramic DIP and a 44-pin leadless ceramic surface mount package and is specified for operation from 0°C to +70°C and −55°C to +125°C.

PRODUCT HIGHLIGHTS

The AD872 offers a complete single-chip sampling 12-bit, 10 Msps analog-to-digital conversion function in a 28-pin DIP or 44-pin leadless ceramic surface mount package (LCC).

Low Power—The AD872 at 1.15 W consumes a fraction of the power of presently available hybrids.

Onboard Track-and-Hold (T/H)—The high impedance T/H input eliminates the need for external buffers and can be configured for single ended or differential inputs.

Out of Range (OTR)—The OTR output bit indicates when the input signal is beyond the AD872's input range.

Ease-of-Use—The AD872 is complete with T/H and voltage reference.

REV. A

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 617/329-4700 **Fax: 617/326-8703**

AD872—SPECIFICATIONS

DC SPECIFICATIONS (T_{MIN} to T_{MAX} with AV_{DD} = +5 V, DV_{DD} = +5 V, AV_{SS} = −5 V, f_{SAMPLE} = 10 MHz unless otherwise indicated)

Parameter	J Grade[1]	S Grade[1]	Units
RESOLUTION	12	12	Bits min
MAX CONVERSION RATE	10	10	MHz min
ACCURACY			
Integral Nonlinearity (INL)	±2.5	±2.5	LSB typ
Differential Nonlinearity (DNL)	±0.5	±0.5	LSB typ
No Missing Codes	12	12	Bits Guaranteed
Zero Error (@ +25°C)[2]	±0.75	±0.75	% FSR max
Gain Error (@ +25°C)[2]	±1.25	±1.25	% FSR max
TEMPERATURE DRIFT[3]			
Zero Error	±0.15	±0.30	% FSR max
Gain Error[3, 4]	±0.80	±1.75	% FSR max
Gain Error[3, 5]	±0.25	±0.50	% FSR max
POWER SUPPLY REJECTION[6]			
AV_{DD}, DV_{DD} (+5 V ± 0.25 V)	±0.125	±0.125	% FSR max
AV_{SS} (−5 V ± 0.25 V)	±0.125	±0.125	% FSR max
ANALOG INPUT			
Input Range	±1	±1	Volts max
Input Resistance	50	50	kΩ typ
Input Capacitance	10	10	pF typ
INTERNAL VOLTAGE REFERENCE			
Output Voltage	2.5	2.5	Volts typ
Output Voltage Tolerance	±20	±40	mV max
Output Current (Available for External Loads) (External load should not change during conversion.)	2.0	2.0	mA typ
REFERENCE INPUT RESISTANCE	5	5	kΩ typ
POWER SUPPLIES			
Supply Voltages			
AV_{DD}	+5	+5	V (±5% AV_{DD} Operating)
AV_{SS}	−5	−5	V (±5% AV_{SS} Operating)
DV_{DD}	+5	+5	V (±5% DV_{DD} Operating)
Supply Current			
IAV_{DD}	87	88	mA max (78 mA typ)
IAV_{SS}	147	150	mA max (134 mA typ)
IDV_{DD}	20	21	mA max (15 mA typ)
POWER CONSUMPTION	1.15	1.15	W typ
	1.25	1.3	W max

NOTES

[1]Temperature ranges are as follows: J Grade: 0°C to +70°C, S Grade: −55°C to +125°C.

[2]Adjustable to zero with external potentiometers (See Zero and Gain Error Calibration section).

[3]+25°C to T_{MIN} and +25°C to T_{MAX}.

[4]Includes internal voltage reference error.

[5]Excludes internal reference drift.

[6]Change in Gain Error as a function of the dc supply voltage.

Specifications subject to change without notice.

AC SPECIFICATIONS (T_{MIN} to T_{MAX} with AV_{DD} = +5 V, DV_{DD} = +5 V, AV_{SS} = −5 V, f_{SAMPLE} = 10 Msps, unless otherwise noted)[1]

	J Grade	S Grade	Units
SIGNAL-TO-NOISE AND DISTORTION RATIO (S/N+D)			
f_{INPUT} = 1 MHz	65	64	dB typ
	61	61	dB min
f_{INPUT} = 4.99 MHz	63	63	dB typ
TOTAL HARMONIC DISTORTION (THD)			
f_{INPUT} = 1 MHz	−70	−68	dB typ
	−63	−62	dB max
f_{INPUT} = 4.99 MHz	−66	−65	dB typ
SPURIOUS FREE DYNAMIC RANGE			
f_{INPUT} = 1 MHz	72	72	dB typ
f_{INPUT} = 4.99 MHz	70	70	dB typ
INTERMODULATION DISTORTION (IMD)[2]	70	70	dB typ
FULL POWER BANDWIDTH	70	70	MHz typ
SMALL SIGNAL BANDWIDTH	70	70	MHz typ
APERTURE DELAY	8	8	ns typ
APERTURE JITTER	10	10	ps rms typ
ACQUISITION TO FULL-SCALE STEP	40	40	ns typ
OVERVOLTAGE RECOVERY TIME	40	40	ns typ

NOTES
[1] f_{IN} amplitude = −0.5 dB full scale unless otherwise indicated. All measurements referred to a 0 dB (1 V pk) input signal unless otherwise indicated.
[2] fa = 1.0 MHz, fb = 0.95 MHz with f_{SAMPLE} = 10 MHz, typical value for second and third order products.
Specifications subject to change without notice.

DIGITAL SPECIFICATIONS (T_{MIN} to T_{MAX} with AV_{DD} = +5 V, DV_{DD} = +5 V, AV_{SS} = −5 V unless otherwise noted)

Parameter	Symbol	J, S Grades	Units
LOGIC INPUTS			
High Level Input Voltage	V_{IH}	+2.0	V min
Low Level Input Voltage	V_{IL}	+0.8	V max
High Level Input Current (V_{IN} = DV_{DD})	I_{IH}	±10	μA max
Low Level Input Current (V_{IN} = 0 V)	I_{IL}	±10	μA max
Input Capacitance	C_{IN}	5	pF typ
LOGIC OUTPUTS			
High Level Output Voltage (I_{OH} = 0.5 mA)	V_{OH}	+2.4	V min
Low Level Output Voltage (I_{OL} = 1.6 mA)	V_{OL}	+0.4	V max
Output Capacitance	C_{OUT}	5	pF typ
Leakage (Three-State, LCC Only)	IZ	±10	μA max

Specifications subject to change without notice.

SWITCHING SPECIFICATIONS (T_{MIN} to T_{MAX} with AV_{DD} = +5 V, DV_{DD} = +5 V, AV_{SS} = −5 V; V_{IL} = 0.8 V, V_{IH} = 2.0 V, V_{OL} = 0.4 V and V_{OH} = 2.4 V)

Parameter	Symbol	J, S Grades	Units
Clock Period[1]	t_C	100	ns min
CLOCK Pulse Width High	t_{CH}	45	ns min
CLOCK Pulse Width Low	t_{CL}	45	ns min
Clock Duty Cycle[2]		40	% min (50% typ)
		60	% max
Output Delay	t_{OD}	10	ns min (20 ns typ)
Pipeline Delay (Latency)		3	Clock Cycles max
Data Access Time (LCC Package Only)[3]	t_{DD}	50	ns typ (100 pF Load)
Output Float Delay (LCC Package Only)[3]	t_{HL}	50	ns typ (10 pF Load)

NOTES
[1]Conversion rate is operational down to 10 kHz without degradation in specified performance.
[2]For clock periods of 200 ns or greater, see Clock Input Section.
[3]See Section on Three-State Outputs for timing diagrams and application information.
Specifications subject to change without notice.

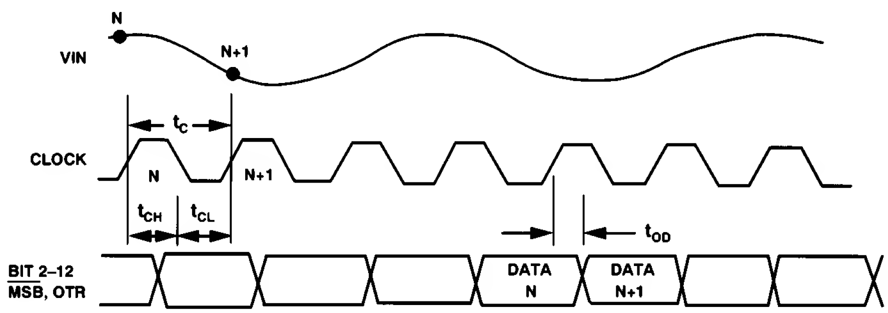


Figure 1. Timing Diagram

ABSOLUTE MAXIMUM RATINGS[1]

Parameter	With Respect to	Min	Max	Units
AV_{DD}	AGND	−0.5	+6.5	Volts
AV_{SS}	AGND	−6.5	+0.5	Volts
DV_{DD}, DRV_{DD}[2]	DGND, DRGND	−0.5	+6.5	Volts
DRV_{DD}[2]	DV_{DD}	−6.5	+6.5	Volts
DRGND[2]	DGND	−0.3	+0.3	Volts
AGND	DGND	−1.0	+1.0	Volts
AV_{DD}	DV_{DD}	−6.5	+6.5	Volts
Clock Input, OEN	DGND	−0.5	DV_{DD} + 0.5	Volts
Digital Outputs	DGND	−0.5	DV_{DD} + 0.3	Volts
V_{INA}, V_{INB} REF IN	AGND	−6.5	+6.5	Volts
REF IN	AGND	AV_{SS}	AV_{DD}	Volts
Junction Temperature			+150	°C
Storage Temperature		−65	+150	°C
Lead Temperature (10 sec)			+300	°C

NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.
[2]LCC Package Only.

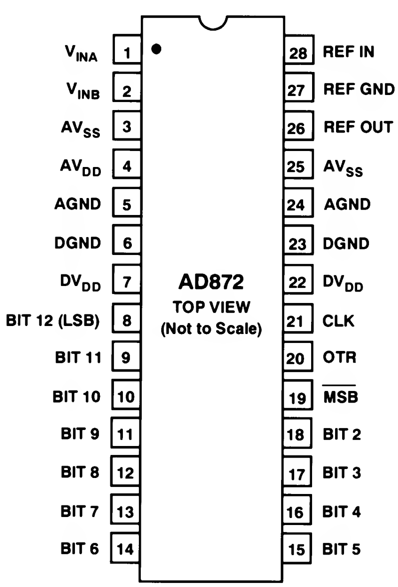
PIN DESCRIPTION

Symbol	DIP Pin No.	LCC Pin No.	Type	Name and Function
AGND	5, 24	9, 36	P	Analog Ground.
AV_{DD}	4	6, 38	P	+5 V Analog Supply.
AV_{SS}	3, 25	5, 40	P	−5 V Analog Supply.
$\overline{MSB}$	19	29	DO	Inverted Most Significant Bit. Provides twos complement output data format.
MSB	N/A	27	DO	Most Significant Bit.
BIT 2–BIT 11	18–9	26–17	DO	Data Bits 2 through 11.
BIT 12 (LSB)	8	16	DO	Least Significant Bit.
CLK	21	31	DI	Clock Input. The AD872 will initiate a conversion on the rising edge of the clock input. See the Timing Diagram for details.
DV_{DD}	7, 22	33	P	+5 V Digital Supply.
DGND	6, 23	10	P	Digital Ground.
DRV_{DD}	N/A	12, 32	P	+5 V Digital Supply for the output drivers.
DRGND	N/A	11, 34	P	Digital Ground for the output drivers. (See section on Power Supply Decoupling for details on DRV_{DD} and DRGND.)
OTR	20	30	DO	Out of Range is Active HIGH on the leading edge of code 0 or the trailing edge of code 4096. See Output Data Format Table III.
OEN	N/A	13	DI	Output Enable. See the Three State Output Timing Diagram for details.
REF GND	27	42	AI	Reference Ground.
REF IN	28	43	AI	Reference Input. +2.5 V input gives ±1 V full-scale range.
REF OUT	26	41	AO	+2.5 V Reference Output. Tie to REF IN for normal operation.
V_{INA}	1	1	AI	(+) Analog Input Signal on the differential input amplifier.
V_{INB}	2	2	AI	(−) Analog Input Signal on the differential input amplifier.
NC	N/A	3, 4, 7, 8, 14, 15 28, 35, 37, 39, 44		No Connect.

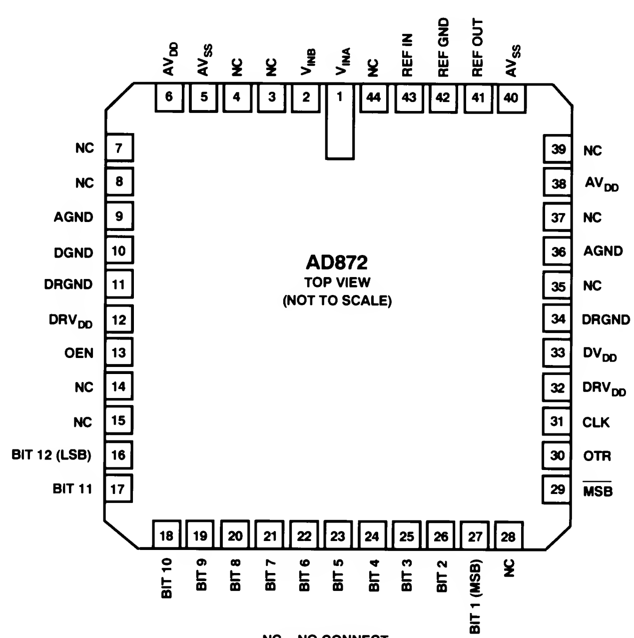
TYPE: AI = Analog Input; AO = Analog Output; DI = Digital Input; DO = Digital Output; P = Power; N/A = Not Available on 28-pin DIP. Only available on 44-pin surface mount package.

PIN CONFIGURATIONS

28-Pin Ceramic DIP



44-Pin LCC



DEFINITIONS OF SPECIFICATIONS

LINEARITY ERROR

Linearity error refers to the deviation of each individual code from a line drawn from "negative full scale" through "positive full scale." The point used as "negative full scale" occurs 1/2 LSB before the first code transition. "Positive full scale" is defined as a level 1 1/2 LSB beyond the last code transition. The deviation is measured from the middle of each particular code to the true straight line.

DIFFERENTIAL LINEARITY ERROR (DNL, NO MISSING CODES)

An ideal ADC exhibits code transitions that are exactly 1 LSB apart. DNL is the deviation from this ideal value. Guaranteed no missing codes to 12-bit resolution indicates that all 4096 codes must be present over all operating ranges.

ZERO ERROR

The major carry transition should occur for an analog value 1/2 LSB below analog common. Zero error is defined as the deviation of the actual transition from that point. The zero error and temperature drift specify the initial deviation and maximum change in the zero error over temperature.

GAIN ERROR

The first code transition should occur for an analog value 1/2 LSB above nominal negative full scale. The last transition should occur for an analog value 1 1/2 LSB below the nominal positive full scale. Gain error is the deviation of the actual difference between first and last code transitions and the ideal difference between first and last code transitions.

TEMPERATURE DRIFT

The temperature drift for zero error and gain error specifies the maximum change from the initial (25°C) value to the value at T_{MIN} or T_{MAX}.

POWER SUPPLY REJECTION

The specifications show the maximum change in the converter's full scale as the supplies are varied from nominal to min/max values.

APERTURE JITTER

Aperture jitter is the variation in aperture delay for successive samples and is manifested as noise on the input to the A/D.

APERTURE DELAY

Aperture delay is a measure of the Track-and-Hold Amplifier (THA) performance and is measured from the rising edge of the clock input to when the input signal is held for conversion.

OVERVOLTAGE RECOVERY TIME

Overvoltage recovery time is defined as that amount of time required for the ADC to achieve a specified accuracy after an overvoltage (50% greater than full-scale range), measured from the time the overvoltage signal reenters the converter's range.

DYNAMIC SPECIFICATIONS

SIGNAL-TO-NOISE AND DISTORTION (S/N+D) RATIO

S/N+D is the ratio of the rms value of the measured input signal to the rms sum of all other spectral components below the Nyquist frequency, including harmonics but excluding dc. The value for S/N+D is expressed in decibels.

TOTAL HARMONIC DISTORTION (THD)

THD is the ratio of the rms sum of the first six harmonic components to the rms value of the measured input signal and is expressed as a percentage or in decibels.

INTERMODULATION DISTORTION (IMD)

With inputs consisting of sine waves at two frequencies, fa and fb, any device with nonlinearities will create distortion products, of order (m + n), at sum and difference frequencies of mfa ± nfb, where m, n = 0, 1, 2, 3 . . . . Intermodulation terms are those for which m or n is not equal to zero. For example, the second order terms are (fa + fb) and (fa − fb), and the third order terms are (2 fa + fb), (2 fa − fb), (fa + 2 fb) and (2 fb − fa). The IMD products are expressed as the decibel ratio of the rms sum of the measured input signals to the rms sum of the distortion terms. The two signals are of equal amplitude and the peak value of their sums is −0.5 dB from full scale. The IMD products are normalized to a 0 dB input signal.

FULL-POWER BANDWIDTH

The full-power bandwidth is that input frequency at which the amplitude of the reconstructed fundamental is reduced by 3 dB for a full-scale input.

SPURIOUS FREE DYNAMIC RANGE

The difference, in dB, between the rms amplitude of the input signal and the peak spurious signal.

ORDERING GUIDE

Model	Temperature Range	Package Option[1]
AD872JD	0°C to +70°C	D-28
AD872JE	0°C to +70°C	E-44A
AD872SD[2]	−55°C to +125°C	D-28
AD872SE[2]	−55°C to +125°C	E-44A

NOTES
[1]D = Ceramic DIP, E = Leadless Ceramic Chip Carrier.
[2]MIL-STD-883 and SMD versions available; contact factory.

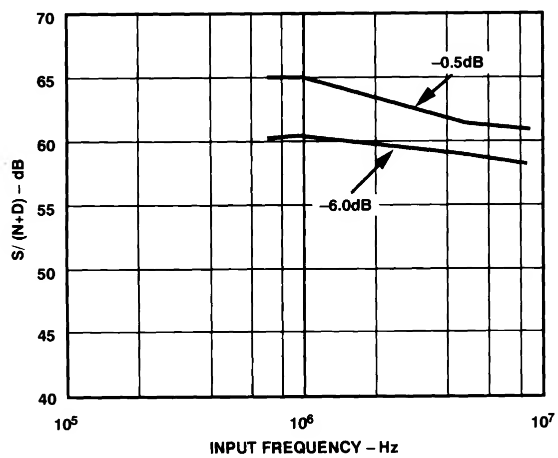


Figure 2. AD872 S/(N+D) vs. Input Frequency

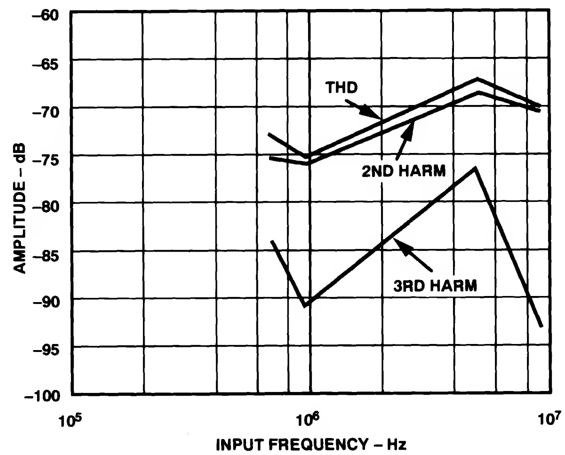


Figure 3. AD872 Distortion vs. Input Frequency, Full-Scale Input

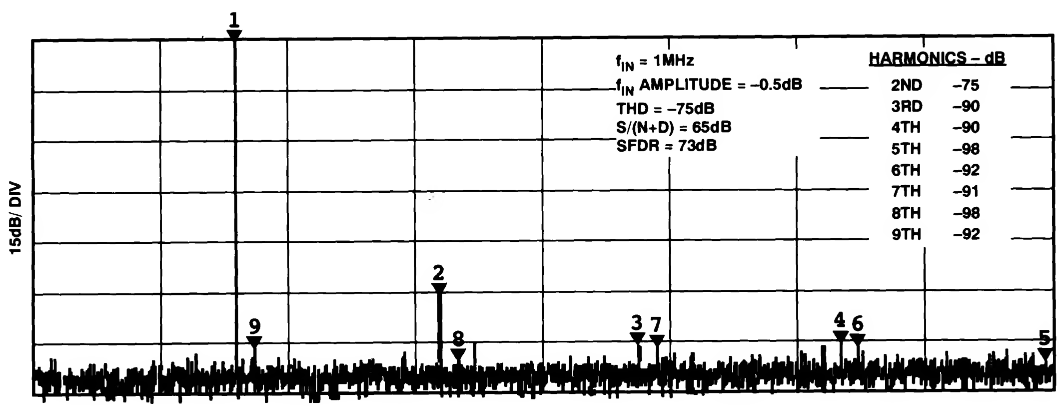


Figure 4. AD872 Typical FFT, f_{IN} = 1 MHz

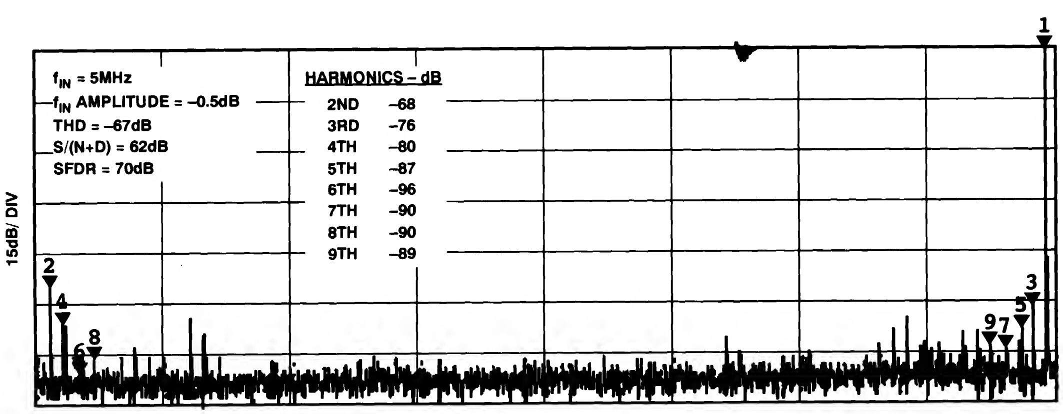


Figure 5. AD872 Typical FFT, f_{IN} = 5 MHz

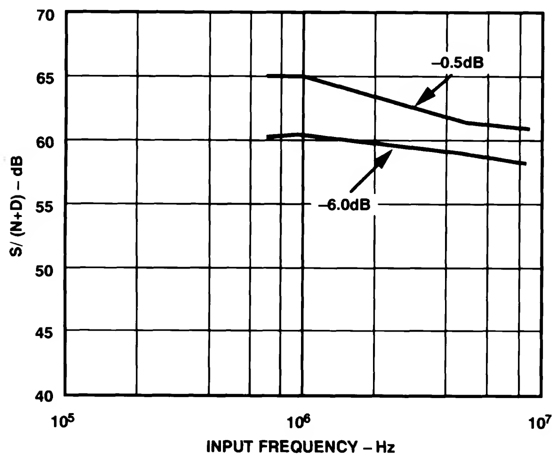


Figure 2. AD872 S/(N+D) vs. Input Frequency

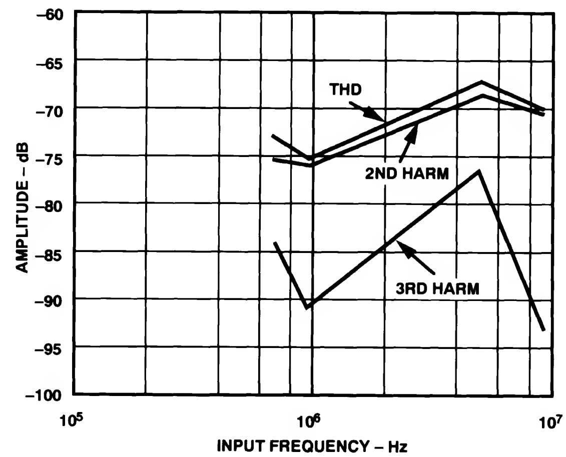


Figure 3. AD872 Distortion vs. Input Frequency, Full-Scale Input

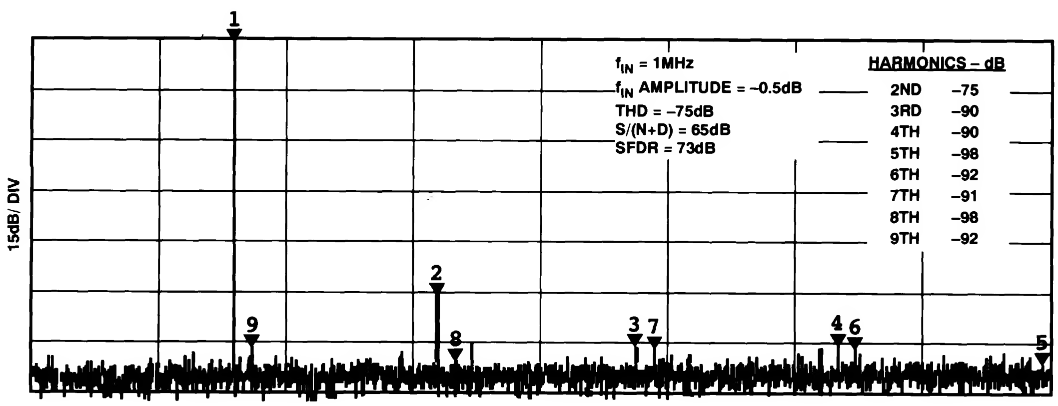


Figure 4. AD872 Typical FFT, f_{IN} = 1 MHz

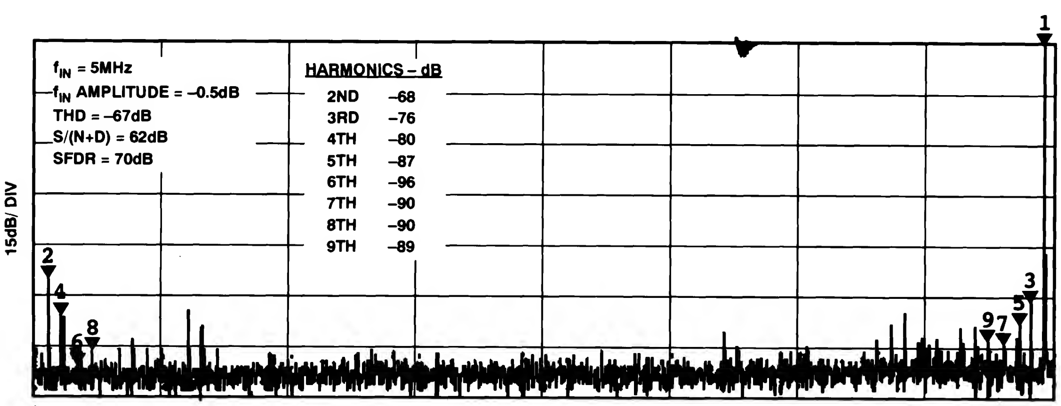


Figure 5. AD872 Typical FFT, f_{IN} = 5 MHz

THEORY OF OPERATION

The AD872 is implemented using a 4-stage pipelined multiple flash architecture. A differential input track-and-hold amplifier (THA) acquires the input and converts the input voltage into a differential current. A 3-bit approximation of the input is made by the first flash converter, and an accurate analog representation of this 3-bit guess is generated by a digital-to-analog converter. This approximation is subtracted from the THA output to produce a remainder, or residue. This residue is then sampled and held by the second THA, and a 4-bit approximation is generated and subtracted by the second stage. Once the second THA goes into hold, the first stage goes back into track to acquire a new input signal. The third stage provides another 4-bit approximation/subtraction operation, and produces the final residue, which is passed to a final 4-bit flash converter. The 15 output bits from the 4 flash converters are accumulated in the correction logic block, which adds the bits together using the appropriate correction algorithm, to produce the 12-bit output word. The digital output, together with overrange indicator, is latched into an output buffer to drive the output pins.

The additional THA inserted in each stage of the AD872 architecture allows pipelining of the conversion. In essence, the converter is converting multiple inputs simultaneously, processing them through the converter chain serially. This means that while the converter is capable of capturing a new input sample every clock cycle, it actually takes three clock cycles for the conversion to be fully processed and appear at the output. This "pipeline delay" is often referred to as latency, and is not a concern in most applications, however there are some cases where it may be a consideration. For example, some applications call for the A/D converter to be placed in a high speed feedback loop, where its input is servoed to provide a desired result at the digital output (e.g., offset calibration or zero restoration in video applications). In these cases the 3 clock cycle delay through the pipeline must be accounted for in the loop stability calculations. Also, because the converter is working on three conversions simultaneously, major disruptions to the part (such as a large glitch on the supplies or reference) may corrupt three data samples. Finally, there will be a minimum clock rate below which the THA droop corrupts the signal in the pipeline. In the case of the AD872, this minimum clock rate is 10 kHz.

The high impedance differential inputs of the AD872 allow a variety of input configurations (see APPLYING THE AD872). The AD872 converts the voltage difference between the V_{INA} and V_{INB} pins. For single-ended applications, one input pin (V_{INA} or V_{INB}) may be grounded, but even in this case the differential input can provide a performance boost: for example, for an input coming from a coaxial cable, V_{INB} can be tied to the shield ground, allowing the AD872 to reject shield noise as common mode. The high input impedance of the device minimizes external driving requirements and allows the user to externally select the appropriate termination impedance for the application.

The AD872 clock circuitry uses both edges of the clock in its internal timing circuitry (see spec page for exact timing requirements.) The AD872 samples the analog input on the rising edge of the clock input. During the clock low time (between the falling edge and rising edge of the clock) the input THA is in track mode; during the clock high time it is in hold. System disturbances just prior to the rising edge of the clock may cause the part to acquire the wrong value, and should be minimized.

While the part uses both clock edges for its timing, jitter is only a significant issue for the rising edge of the clock (see CLOCK INPUT section).

APPLYING THE AD872

ANALOG INPUTS

The AD872 features a high impedance differential input that can readily operate on either single-ended or differential input signals. Table I summarizes the nominal input voltage span for both single-ended and differential modes, assuming a 2.5 V reference input.

Table I. Input Voltage Span

	V_{INA}	V_{INB}	$V_{INA}-V_{INB}$
Single-Ended	+1 V	GND	+1 V (Positive Full Scale)
	−1 V	GND	−1 V (Negative Full Scale)
Differential	+0.5 V	−0.5 V	+1 V (Positive Full Scale)
	−0.5 V	+0.5 V	−1 V (Negative Full Scale)

Figure 10 shows an approximate model for the analog input circuit. As this model indicates, when the input exceeds 1.6 V (with respect to AGND), the input device may saturate, causing the input impedance to drop substantially and significantly reducing the performance of the part. Input compliance in the negative direction is somewhat larger, showing virtually no degradation in performance for inputs as low as −1.9 V.

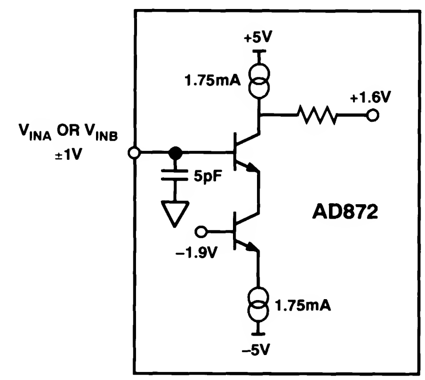


Figure 10. AD872 Equivalent Analog Input Circuit

Figure 11 illustrates the effect of varying the common-mode voltage of a −1 dB input signal on total harmonic distortion.

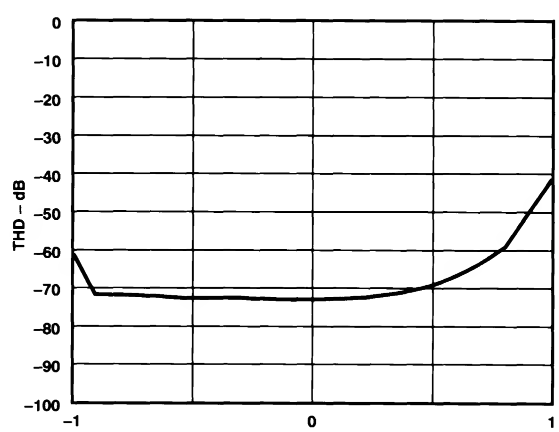


Figure 11. AD872 Total Harmonic Distortion vs. CM Input Voltage, f_{IN} = 1 MHz, FS = 10 MSPS

Figure 12 shows the common-mode rejection performance vs. frequency for a 1 V p-p common mode input. This excellent common-mode rejection out over a wide bandwidth affords the user the opportunity to eliminate many potential sources of input noise as common mode by using the differential input structure of the AD872.

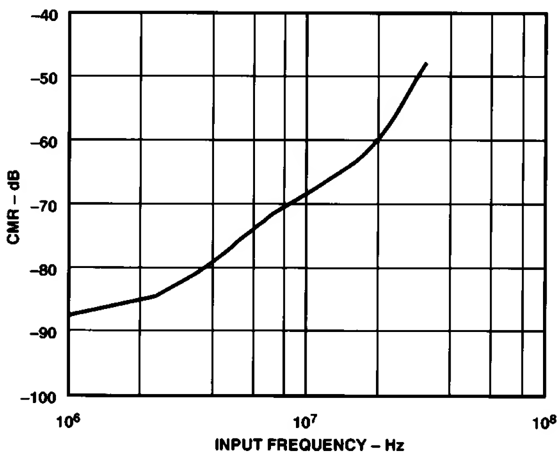


Figure 12. Common-Mode Rejection vs. Input Frequency, 1 V p-p Input

Figures 13 and 14 illustrate typical input connections for single-ended inputs.

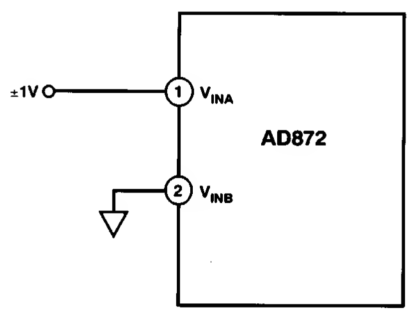


Figure 13. AD872 Single-Ended Input Connection

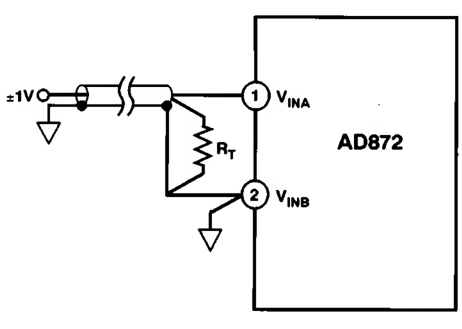


Figure 14. AD872 Single-Ended Input Connection Using a Shielded Cable

The cable shield is used as the ground connection for the V_{INB} input, providing the best possible rejection of the cable noise from the input signal. Note also that the high input impedance of the AD872 allows the user to select his own termination impedance, be it 50 ohms, 75 ohms, or some other value. Furthermore, unlike many flash converters, most AD872 applications will not require an external buffer amplifier. If such an amplifier is required, we suggest either the AD811 or AD9617.

Figure 15 illustrates how external amplifiers may be used to convert a single-ended input into a differential signal. The resistor values of 536 Ω and 562 Ω were selected to provide optimum phase matching between U1 and U2.

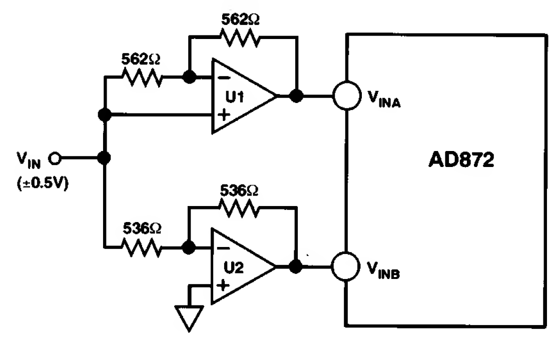


Figure 15. Single-Ended to Differential Connections; U1, U2 = AD811 or AD9617

The use of the differential input signal can help to minimize even-order distortion from the input THA where performance beyond −70 dB is desired.

Figure 16 shows the AD872 large signal (−0.5 dB) and small signal (−20 dB) frequency response.

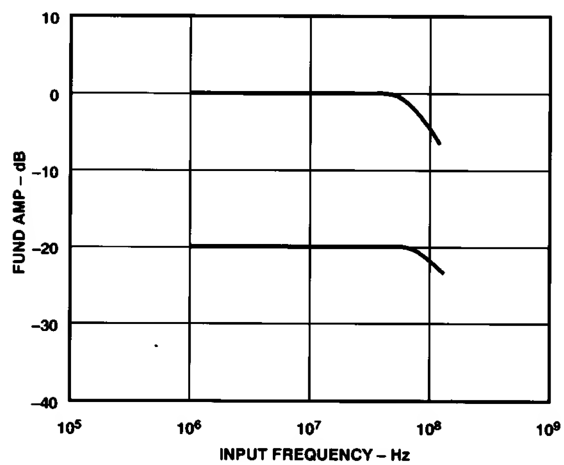


Figure 16. Full Power (−0.5 dB) and Small Signal Response (−20 dB) vs. Input Frequency

The AD872's wide input bandwidth facilitates rapid acquisition of transient input signals: the input THA can typically settle to 12-bit accuracy from a full-scale input step in less than 40 ns. Figure 17 illustrates the typical acquisition of a full-scale input step.

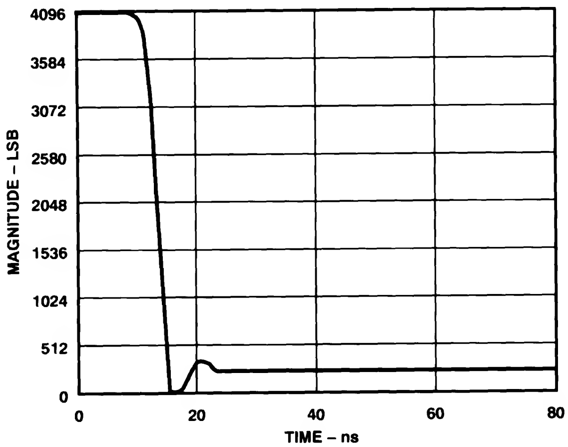


Figure 17. Typical AD872 Settling Time

The wide input bandwidth and superior dynamic performance of the input THA makes the AD872 suitable for undersampling applications where the input frequency exceeds half the sampling frequency. The input THA is designed to recover rapidly from input overdrive conditions, returning from a 50% overdrive in less than 50 ns.

Because of the THA's exceptionally wide input bandwidth, some users may find the AD872 is sensitive to noise at frequencies from 50 MHz to 100 MHz that other converters are incapable of responding to. This sensitivity can be mitigated by careful use of the differential inputs (see previous paragraphs). Additionally, Figure 18 shows how a small capacitor (10 pF–20 pF for 50-ohm terminated inputs) may be placed between V_{INA} and V_{INB} to help reduce high frequency noise in applications where limiting the input bandwidth is acceptable.

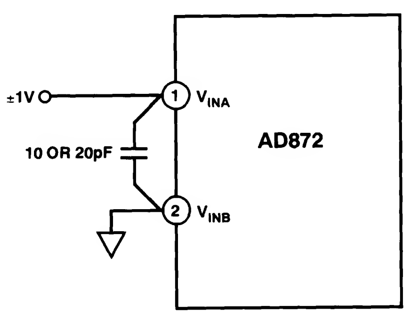


Figure 18. Optional High Frequency Noise Reduction

The AD872 will contribute its own wideband thermal noise. As a result of the integrated wideband noise (1/2 LSB rms, referred-to-input), applying a dc analog input produces more than one code at the output. A histogram analysis of the AD872 with a dc input will show a bell shaped curve consistent with the Guassian nature of the thermal noise. This histogram will be between 3 and 5 codes wide, depending on how well the input is centered on a given code and how many samples are taken.

REFERENCE INPUT

The nominal reference input should be 2.5 V, taken with respect to REFERENCE GROUND (REF GND). Figure 19 illustrates the equivalent model for the reference input: there is no clock or signal-dependent activity associated with the reference input circuitry, therefore, no "kickback" into the reference.

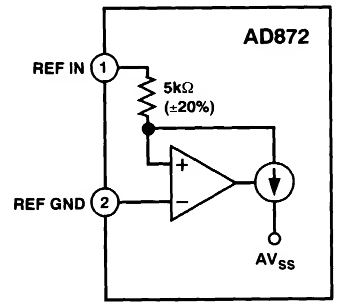


Figure 19. Equivalent Reference Input Circuit

The AD872's input impedance is 5 kΩ, with a tolerance of ±20%. The effective noise bandwidth through the input channel is 10 MHz, and the referred-to-input noise gain is 0.4. For example, the internal reference, with peak-to-peak noise of 180 μV (using an external 1 μF capacitor), contributes 0.3 LSBs of noise to the transfer function of the AD872.

The full-scale peak-to-peak input voltage is a function of the reference voltage, according to the equation:

$$(V_{INA} - V_{INB})\ Full\ Scale = 0.8*(V_{REF} - REF\ GND)$$

Note that the AD872's performance was optimized for a 2.5 V reference input: performance will degrade somewhat for other reference voltages. Figure 20 illustrates the S/(N+D) performance vs. reference voltage for a 1 MHz, −0.5 dB input signal. Note also that if the reference is changed during a conversion, all three conversions in the pipeline will be invalidated.

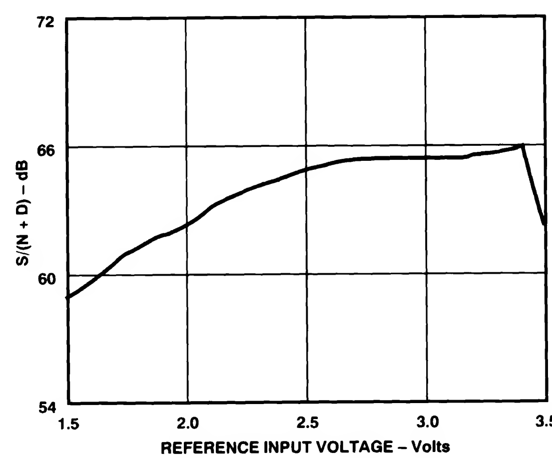


Figure 20. S/(N+D) vs. Reference Input Voltage, f_{IN} = 1 MHz, FS = 10 MHz

Table II summarizes various 2.5 V references suitable for use with the AD872, including the onboard bandgap reference (see REFERENCE OUTPUT section).

Table II. Suitable 2.5 V References

	Drift (PPM/°C)	Initial Accuracy %
REF-43B	6 (max)	0.2
AD680JN	10 (max)	0.4
Internal	30 (typ)	0.4

If an external reference is connected to REF IN, REF OUT must be connected to +5 V. This should lower the current in REF GND to less than 350 μA, and eliminate the need for a 1 μF capacitor.

Alternatively, Figure 21 shows how the AD872 may be driven from other references by use of an external resistor. The external resistor forms a resistor divider with the on-chip 5 kΩ resistor to realize 2.5 V at the reference input pin (REF IN). A trim potentiometer is recommended to accommodate the tolerance of the AD872's 5 kΩ resistor.

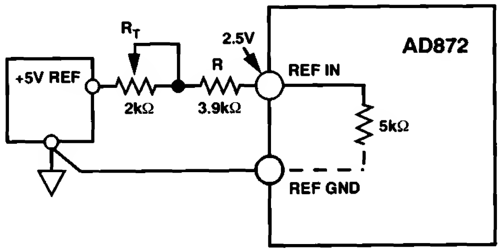


Figure 21. Optional +5 V Reference Input Circuit

REFERENCE GROUND

The REF GND pin provides the reference point for both the reference input, and the reference output. When the internal reference is operating, it will draw approximately 500 μA of current through the reference ground, so a low impedance path to the external common is desirable. The AD872 can tolerate a fairly large difference between REF GND and AGND, up to ±1 V, without any performance degradation.

REFERENCE OUTPUT

The AD872 features an onboard, curvature compensated bandgap reference that has been laser trimmed for both absolute value and temperature drift. The output stage of the reference was designed to allow the use of an external capacitor to limit the wideband noise. As Figure 22 illustrates, *a 1 μF capacitor on the reference output is required for stability of the reference output buffer*. Note: If used, an external reference may become unstable with this capacitor in place.

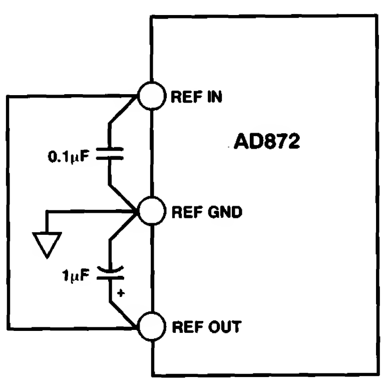


Figure 22. Typical Reference Decoupling Connection

With this capacitor in place, the noise on the reference output is approximately 30 μV rms at room temperature. Figure 23 shows the typical temperature drift performance of the reference, while Figure 24 illustrates the variation in reference voltage with load currents.

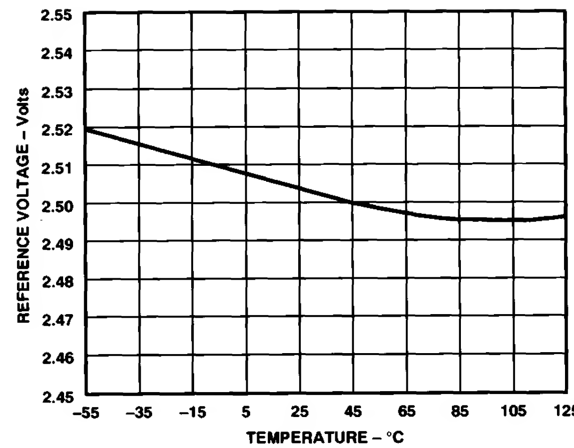


Figure 23. Reference Output Voltage vs. Temperature

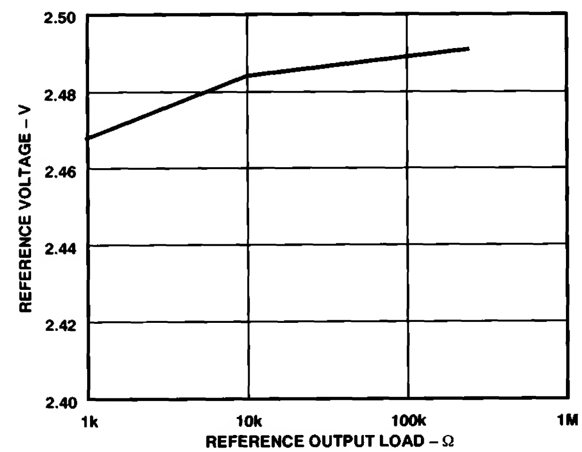


Figure 24. Reference Output Voltage vs. Output Load

The output stage is designed to provide at least 2 mA of output current, allowing a single reference to drive up to four AD872s, or other external loads. The power supply rejection of the reference is better than 54 dB at dc.

DIGITAL OUTPUTS

In 28-pin packages, the AD872 output data is presented in twos complement format. Table III indicates offset binary and twos complement output for various analog inputs.

Table III. Output Data Format

Analog Input	Digital Output		
V_{INA}–V_{INB}	Offset Binary	Twos Complement	OTR
≥0.999756 V	1111 1111 1111	0111 1111 1111	1
0.999268 V	1111 1111 1111	0111 1111 1111	0
0 V	1000 0000 0000	0000 0000 0000	0
−1 V	0000 0000 0000	1000 0000 0000	0
−1.000244 V	0000 0000 0000	1000 0000 0000	1

Users requiring offset binary encoding may simply invert the $\overline{\text{MSB}}$ pin. In the 44-pin surface mount packages, both MSB and $\overline{\text{MSB}}$ bits are provided.

The AD872 features a digital out-of-range (OTR) bit that goes high when the input exceeds positive full scale or falls below negative full scale. As Table III indicates, the output bits will be

set appropriately according to whether it is an out-of-range high condition or an out-of-range low condition.

The AD872's CMOS digital output drivers are sized to provide sufficient output current to drive a wide variety of logic families. However, large drive currents tend to cause glitches on the supplies and may affect S/(N+D) performance. Applications requiring the AD872 to drive large capacitive loads or large fanout may require additional decoupling capacitors on DRV_{DD} and DV_{DD}. In extreme cases, external buffers or latches could be used.

THREE-STATE OUTPUTS

The 44-pin surface mount AD872 offers three-state outputs. The digital outputs can be placed into a three-state mode by pulling the OUTPUT ENABLE (OEN) pin LOW. Note that this function is not intended to be used to pull the AD872 on and off a bus at 10 MHz. Rather, it is intended to allow the ADC to be pulled off the bus for evaluation or test modes. Also, to avoid corruption of the sampled analog signal during conversion (3 clock cycles), it is highly recommended that the AD872 be placed on the bus prior to the first sampling.

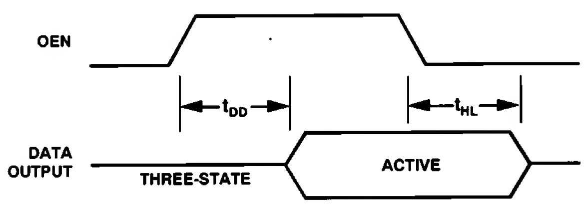


Figure 25. Three-State Output Timing Diagram

For timing budgetary purposes, the maximum access and float delay times for the AD872 are 200 ns.

CLOCK INPUT

The AD872 internal timing control uses the two edges of the clock input to generate a variety of internal timing signals. The optimal clock input should have a 50% duty cycle; however, sensitivity to duty cycle is significantly reduced for clock rates of less than 10 megasamples per second.

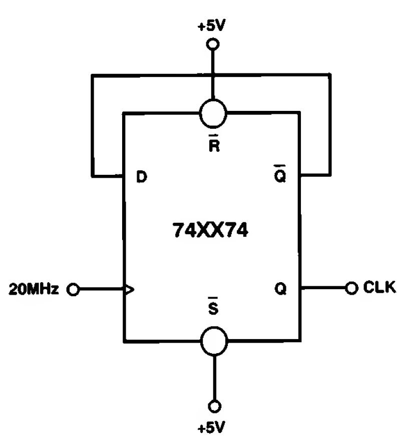


Figure 26. Divide-by-Two Clock Circuit

Due to the nature of on-chip compensation circuitry, the duty cycle should be maintained between 40% and 60% even for clock rates less than 10 Msps. One way to realize a 50% duty cycle clock is to divide down a clock of higher frequency, as shown in Figure 26.

In this case, a 20 MHz clock is divided by 2 to produce the 10 MHz clock input for the AD872. In this configuration, the duty cycle of the 20 MHz clock is irrelevant.

The input circuitry for the CLKIN pin is designed to accommodate both TTL and CMOS inputs. The quality of the logic input, particularly the rising edge, is critical in realizing the best possible jitter performance for the part: the faster the rising edge, the better the jitter performance.

As a result, careful selection of the logic family for the clock driver, as well as the fanout and capacitive load on the clock line, is important. Jitter-induced errors become more predominant at higher frequency, large amplitude inputs, where the input slew rate is greatest.

The AD872 is designed to support a sampling rate of 10 Msps; running at slightly faster clock rates may be possible, although at reduced performance levels. Conversely, some slight performance improvements might be realized by clocking the AD872 at slower clock rates. Figure 27 presents the SNR vs. clock frequency for a 1 MHz analog input.

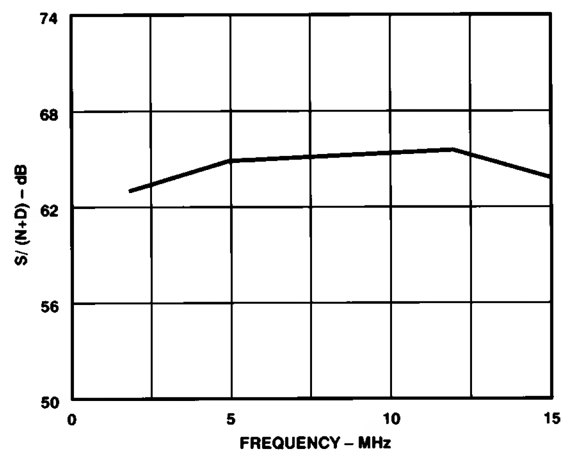


Figure 27. Typical S/(N+D) vs. Clock Frequency f_{IN} = 1 MHz, Full-Scale Input

The power dissipated by the correction logic and output buffers is largely proportional to the clock frequency; running at reduced clock rates provides a slight reduction in power consumption. Figure 28 illustrates this tradeoff.

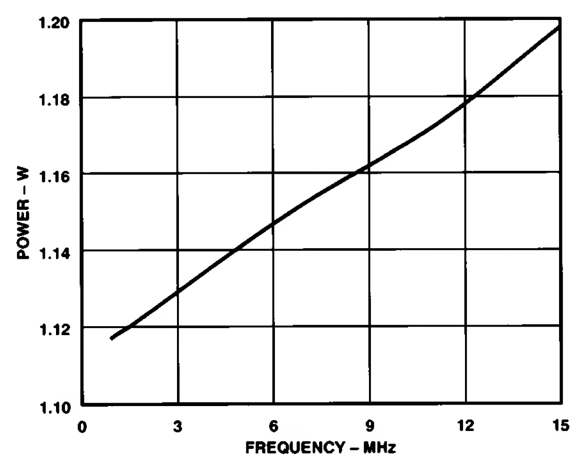


Figure 28. Typical Power Dissipation vs. Clock Frequency

ANALOG SUPPLIES AND GROUNDS

The AD872 features separate analog and digital supply and ground pins, helping to minimize digital corruption of sensitive analog signals. In general, AV_{SS} and AV_{DD}, the analog supplies, should be decoupled to AGND, the analog common, as close to the chip as physically possible. Care has been taken to minimize the signal dependence of the power supply currents; however, the analog supply currents will be proportional to the reference input. With REFIN at 2.5 V, the typical current into AV_{DD} is 78 mA, while the typical current out of AV_{SS} is 134 mA. Typically, 55 mA will flow into the AGND pin.

Careful design and the use of differential circuitry provide the AD872 with excellent rejection of power supply noise over a wide range of frequencies, as illustrated in Figure 29.

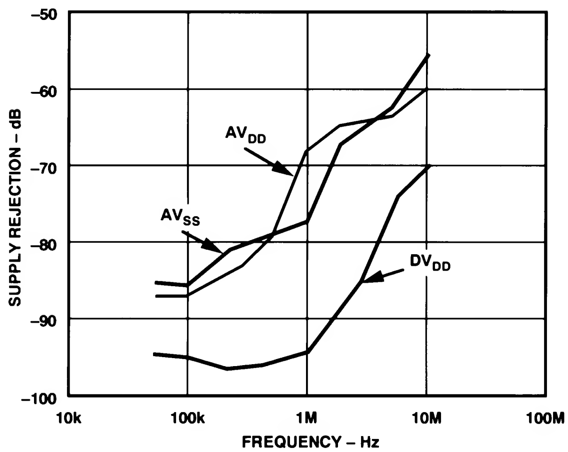


Figure 29. Power Supply Rejection vs. Frequency, 100 mV p-p Signal on Power Supplies

Figure 30 shows the degradation in SNR ratio resulting from 100 mV of power supply ripple at various frequencies. As Figure 30 shows, careful decoupling is required to realize the specified dynamic performance. Figure 35 demonstrates the recommended decoupling strategy for the supply pins. Note that in extremely noisy environments, a more elaborate supply filtering scheme may be necessary.

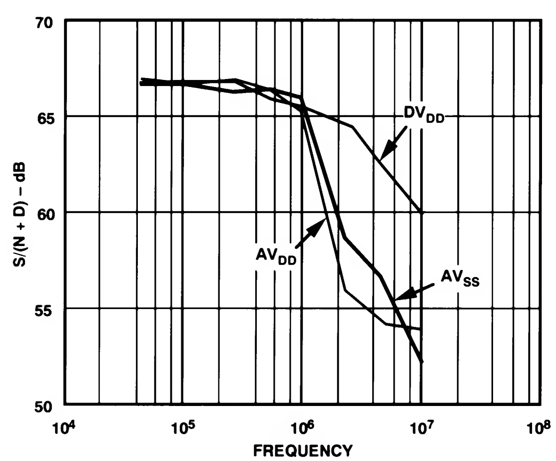


Figure 30. SNR vs. Supply Noise Frequency (f_{IN} = 1 MHz)

DIGITAL SUPPLIES AND GROUNDS

The digital activity on the AD872 chip falls into two general categories: CMOS correction logic, and CMOS output drivers. The internal correction logic draws relatively small surges of current, mainly during the clock transitions; in the 44-pin package, these currents flow through pins DGND and DV_{DD}. The output drivers draw large current impulses while the output bits are changing. The size and duration of these currents is a function of the load on the output bits: large capacitive loads are to be avoided. In the 44-pin package, the output drivers are supplied through dedicated pins DRGND and DRV_{DD}. Pin count constraints in the 28-pin packages require that the digital and driver supplies share package pins (although they have separate bond wires and on-chip routing). The decoupling shown in Figure 35 is appropriate for a reasonable capacitive load on the digital outputs (typically 20 pF on each pin). Applications involving greater digital loads should consider increasing the digital decoupling proportionately.

APPLICATIONS

OPTIONAL ZERO AND GAIN TRIM

The AD872 is factory trimmed to minimize zero error, gain error and linearity errors. In some applications the zero and gain errors of the AD872 need to be externally adjusted to zero. If required, both zero error and gain error can be trimmed with external potentiometers as shown in Figure 31. Note that gain error adjustments must be made with an external reference.

Zero trim should be adjusted first. Connect V_{INA} to ground and adjust the 10 kΩ potentiometer such that a nominal digital output code of 0000 0000 0000 (twos complement output) exists. Note that the zero trim should be decoupled and that the accuracy of the ±2.5 V reference signals will directly affect the offset.

Gain error may then be calibrated by adjusting the REF IN voltage. The REF IN voltage should be adjusted such that a +1 V input on V_{INA} results in the digital output code 01111 1111 1111 (twos complement output).

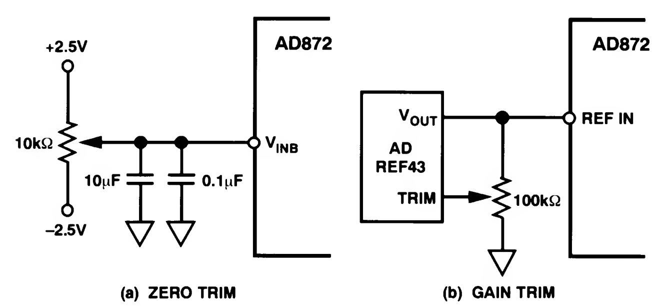


Figure 31. Zero and Gain Error Trims

DIGITAL OFFSET CORRECTION

The AD872 provides differential inputs that may be used to correct for any offset voltages on the analog input. For applications where the input signal contains a dc offset, it may be advantageous to apply a nulling voltage to the V_{INB} input. Applying a voltage equal to the dc offset will maximize the full-scale input range and therefore the dynamic range. Offsets ranging from −0.7 V to +0.5 V can be corrected.

Figure 32 shows how a dc offset can be applied using the AD568 12-bit, high speed digital-to-analog converter (DAC). This circuit can be used for applications requiring offset adjustments on every clock cycle. The AD568 connection scheme is used to provide a −0.512 V to +0.512 V output range. The offset voltage must be stable on the rising edge of the AD872 clock input.

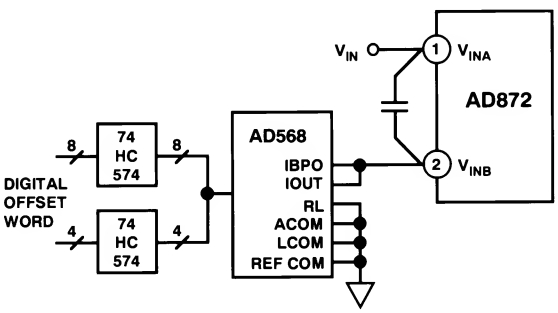


Figure 32. Offset Correction Using the AD568

UNDERSAMPLING USING THE AD872 and AD9100

The AD872's on-chip THA optimizes transient response while maintaining low noise performance. For super-Nyquist (undersampling) applications it may be necessary to use an external THA with fast track-mode slew rate and hold mode settling time. An excellent choice for this application is the AD9100, an ultrahigh speed track-and-hold amplifier.

In order to maximize the spurious free dynamic range of the circuit in Figure 33 it is advantageous to present a small signal to the input of the AD9100 and then amplify the output to the AD872's full-scale input range. This can be accomplished with a low distortion, wide bandwidth amplifier such as the AD9617. The circuit uses a gain of 3.5 to optimize S/(N+D).

The performance of this circuit configuration is compared with the AD872 by itself in Figure 34. This shows that peak performance is obtained by driving the AD872 + AD9100 combination with a full-scale input. At −20 dB and −40 dB signal levels, the AD872 performs better without the track-and-hold because slew-limiting effects are no longer dominant. To gain the advantages of the added track-and-hold, it is important to give the AD872 a full-scale input.

An alternative to the configuration presented above is to use the AD9101 track-and-hold amplifier. The AD9101 provides a built-in post amplifier with a gain of 4, providing excellent ac characteristics in conjunction with a high level of integration.

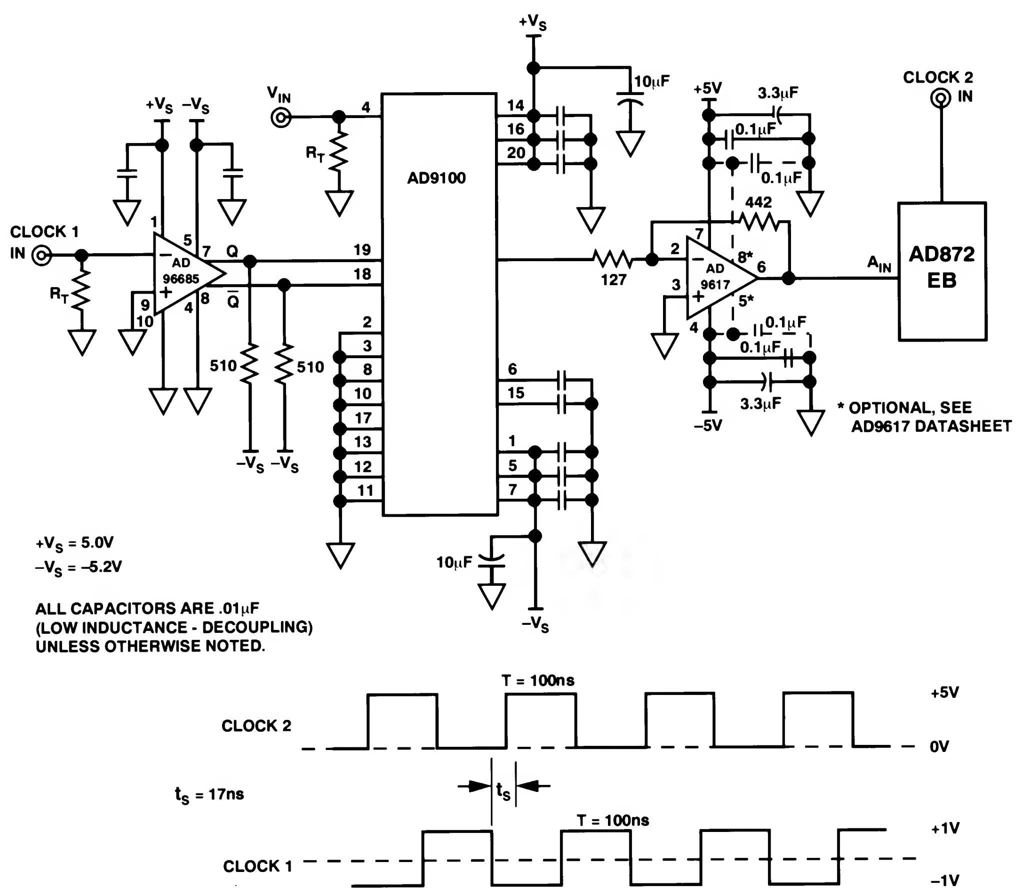


Figure 33. Undersampling Using the AD872 and AD9100

As illustrated in Figure 33, it is necessary to skew the AD872 sample clock and the AD9100 sample/hold control. Clock skew (t_S) is defined as the time starting at the AD9100's transition into hold mode and ending at the moment the AD872 samples. The AD872 samples on the rising edge of the sample clock, and the AD9100 samples on the falling edge of the sample/hold control. The choice of t_S is primarily determined by the settling time of the AD9100. The droop rate of the AD9100 must also be taken into consideration. Using these values, the ideal t_S is 17 ns. When choosing clock sources, it is extremely important that the front end track-and-hold sample/hold control is given a very low jitter clock source. This is not as crucial for the AD872 sample clock, because it is sampling a dc signal.

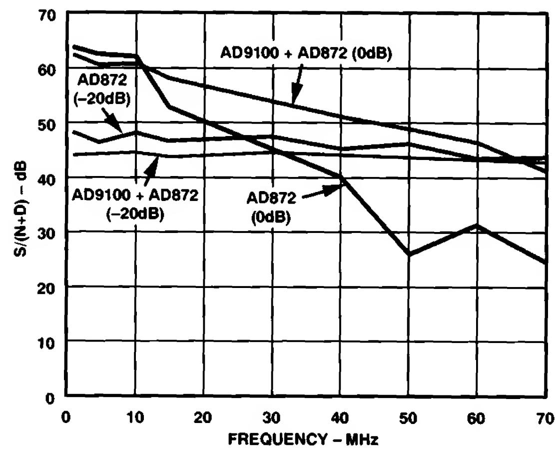


Figure 34. Typical S/(N+D) vs. Input Frequency for the Circuit in Figure 33

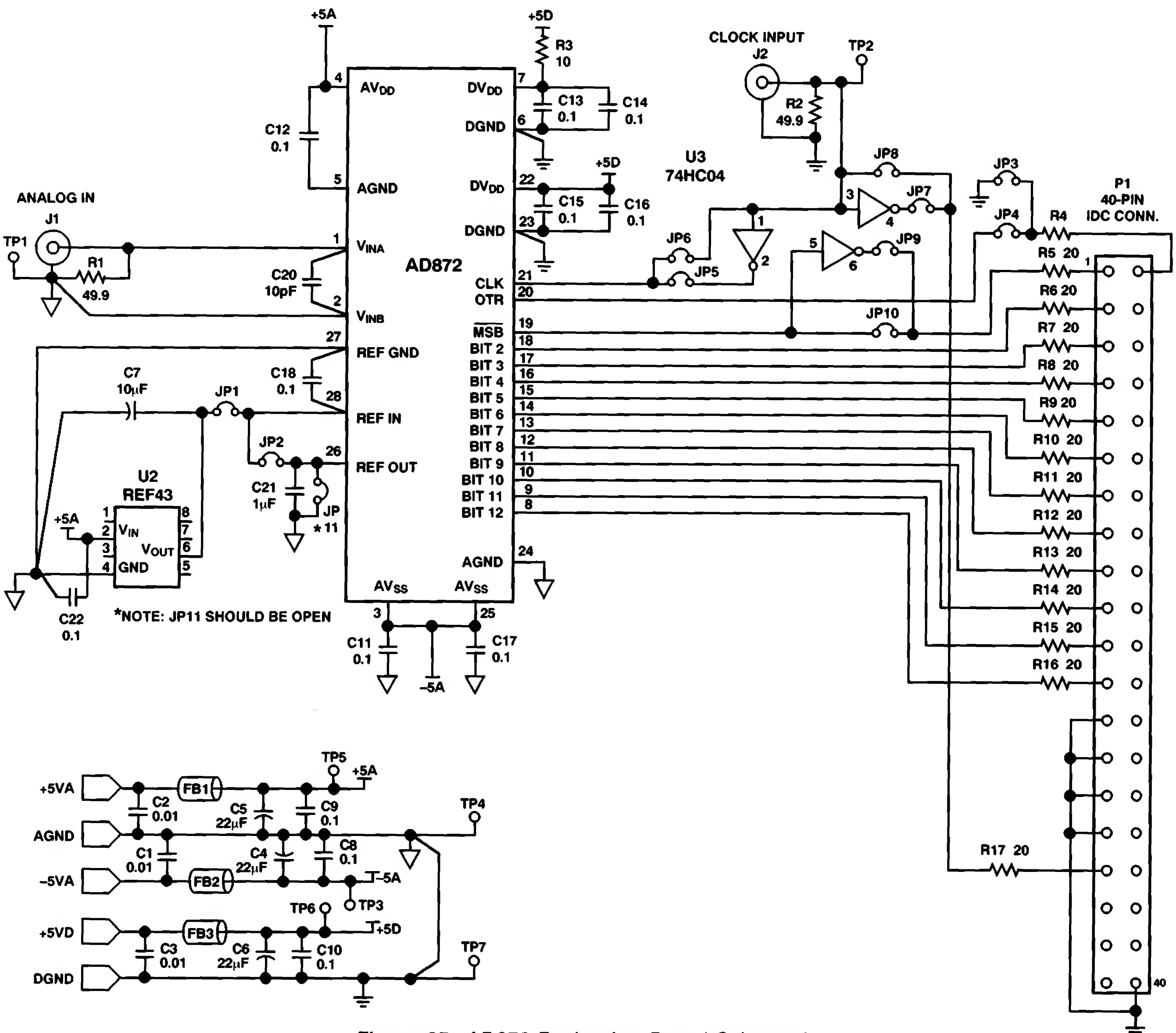


Figure 35. AD872 Evaluation Board Schematic

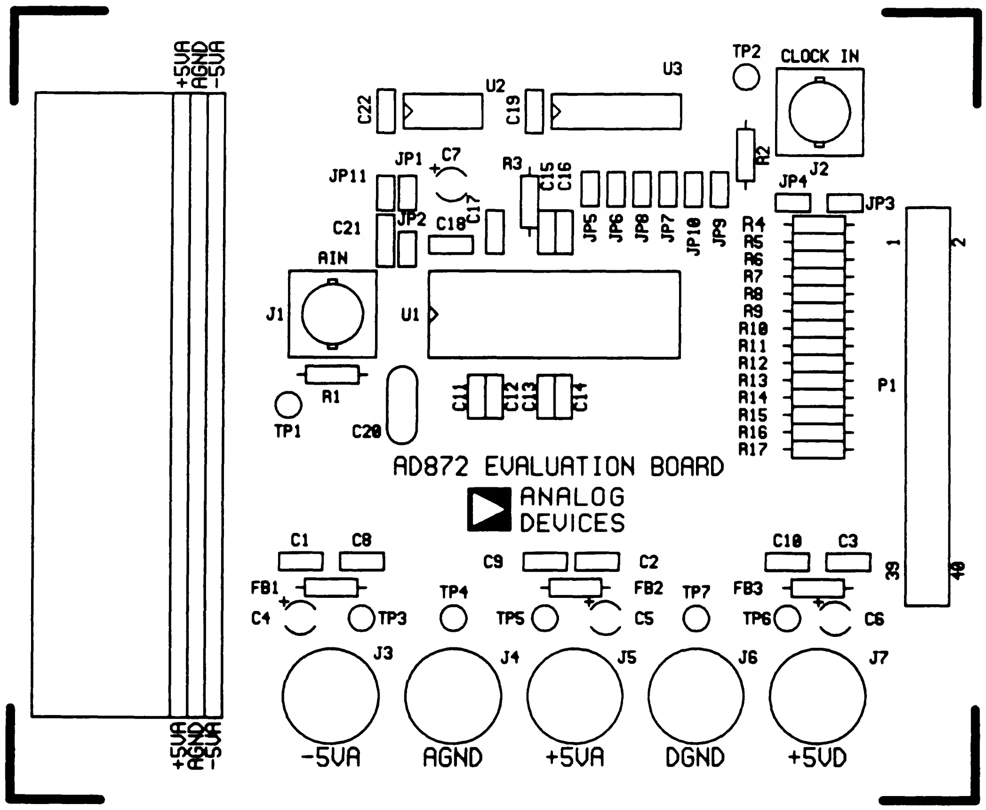


Figure 36. Silkscreen Layer PCB Layout (Not Shown to Scale)

Table IV. Components List

Reference Designator	Description	Quantity
R1, R2	Resistor, 1%, Metal Film, 49.9 Ω	2
R3	Resistor, 1%, Metal Film, 10	1
R4–R17	Resistor, 1%, Metal Film, 20	14
C1–C3	SMD Chip Capacitor, 0.01 μF	3
C4–C6	Capacitor, Tantalum, 22 μF	3
C7	Capacitor, Tantalum, 10 μF	1
C8–C19, C22	SMD Chip Capacitor, 0.1 μF	13
C20	Capacitor, Mica, 10 pF	1
C21	Capacitor, Ceramic, 1 μF	1
U1	AD872	1
U2	REF-43B	1
U3	74HC04N	1
FB1–FB3	Ferrite Bead	3
J1, J2	BNC Jack	2
JP2, 3, 5, 7, 10	Jumpers	5
JP1–JP11	Headers	11
P1	40-Pin IDC Connector	1

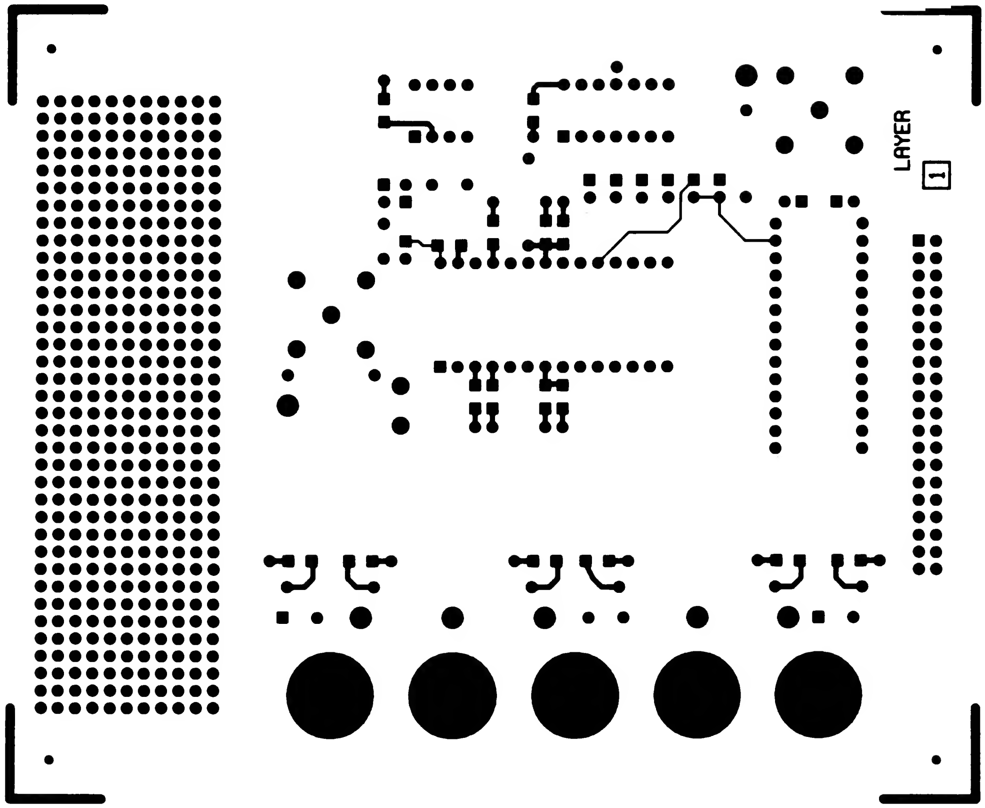


Figure 37. Component Side PCB Layout (Not Shown to Scale)

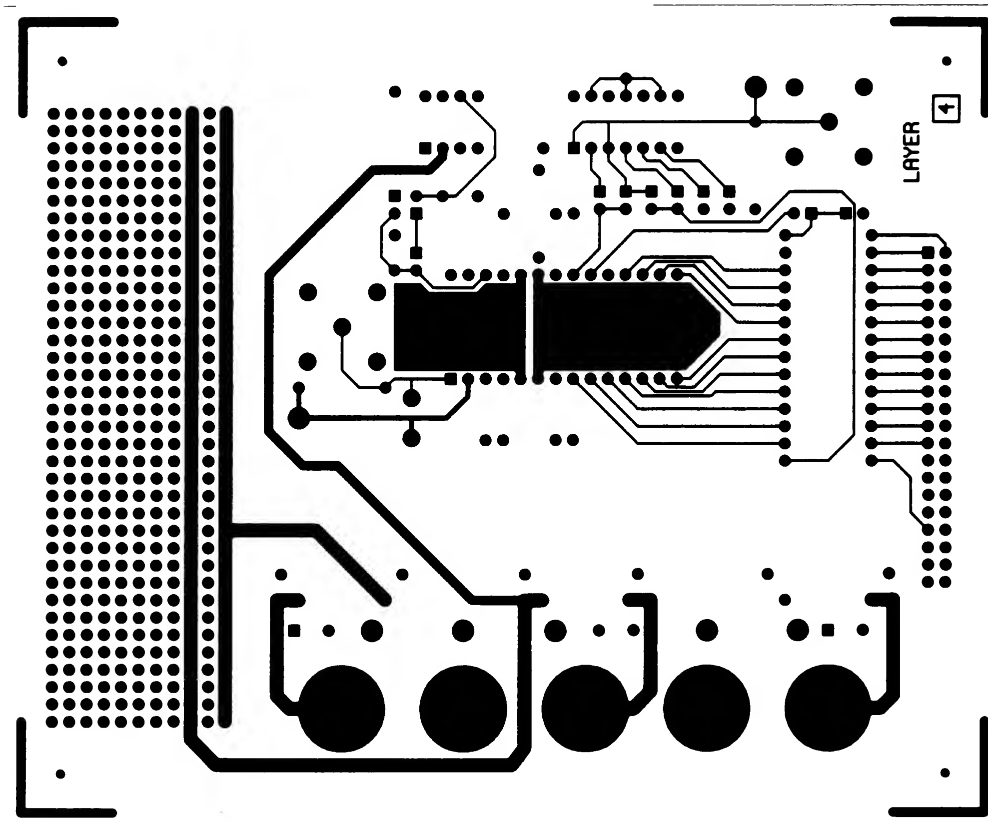


Figure 38. Solder Side PCB Layout (Not Shown to Scale)

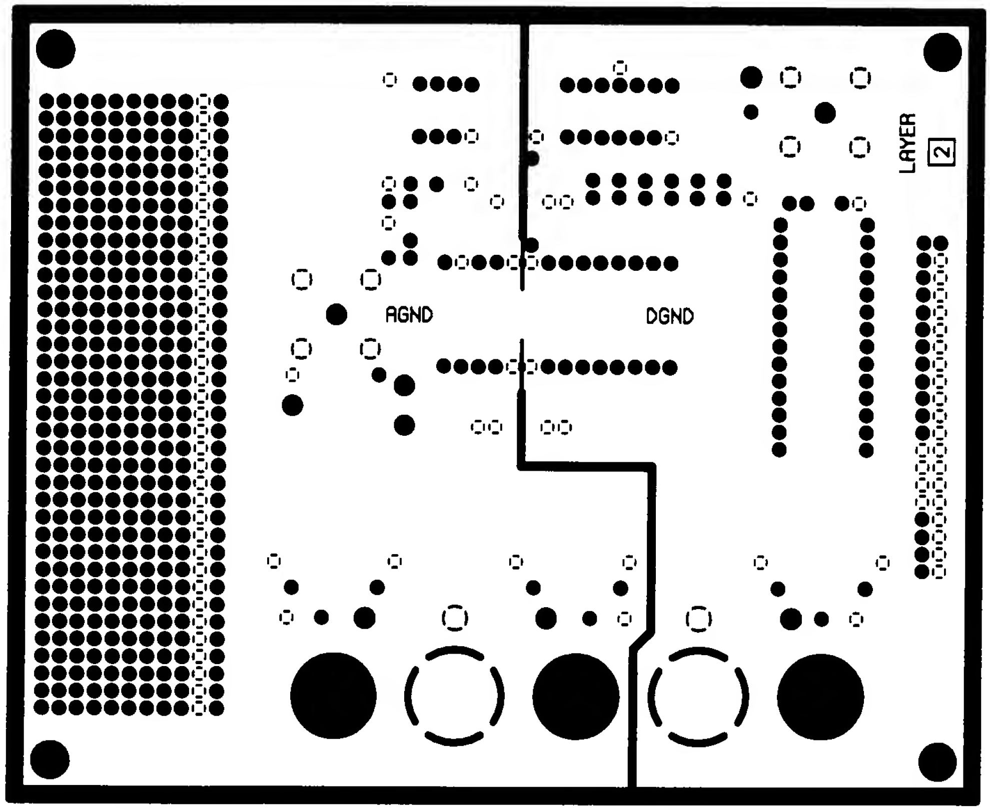


Figure 39. Ground Layer PCB Layout (Not Shown to Scale)

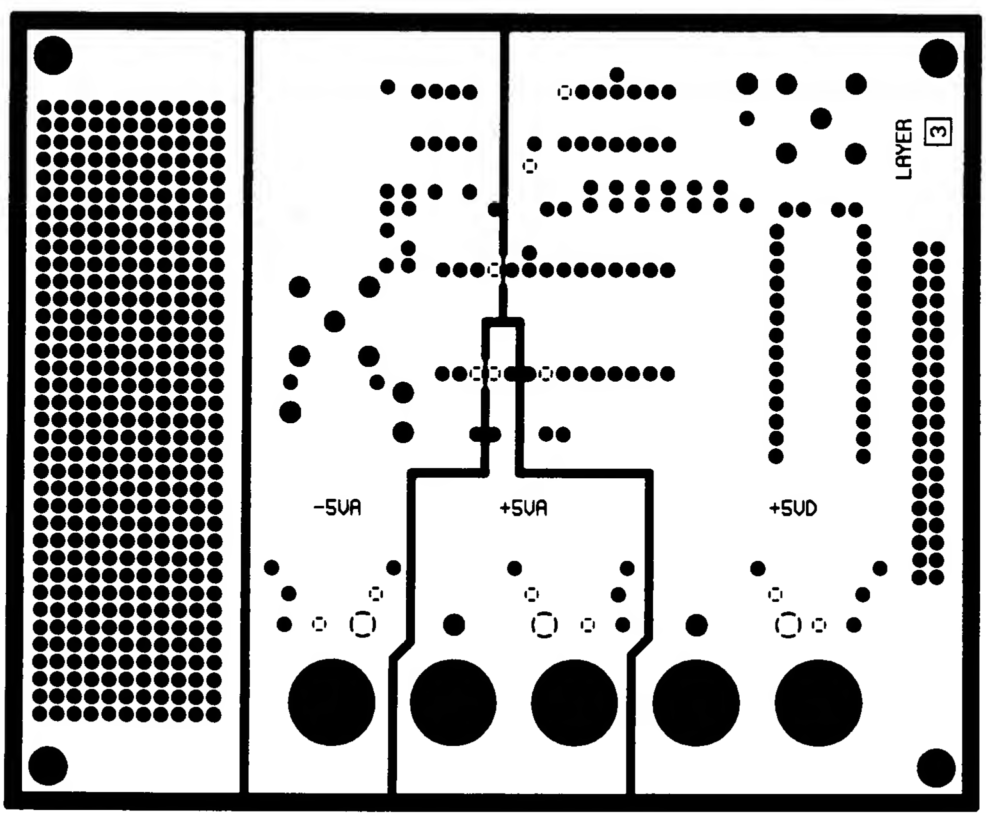
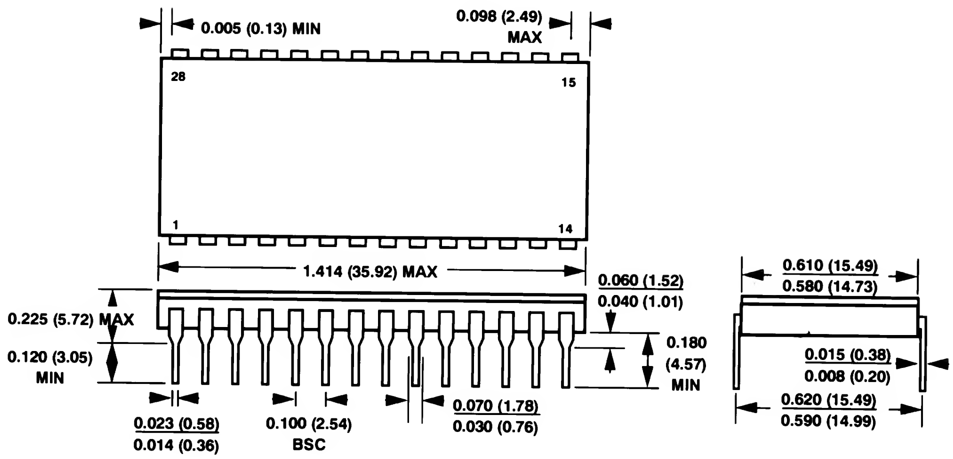


Figure 40. Power Layer PCB Layout (Not Shown to Scale)

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

28-Pin Sidebrazed DIP (D-28)



44-Pin LCC (E-44A)